UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,836	04/12/2004	Sandeep Pant	20-336	1754

7590 05/27/2008

MANELLI DENISON & SELTER PLLC
2000 M Street, N.W.
7th Floor
Washington, DC 20036-3307

EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	
ART UNIT	PAPER NUMBER
2836	
MAIL DATE	DELIVERY MODE
05/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,836	PANT ET AL.	
	Examiner	Art Unit	
	TERRENCE R. WILLOUGHBY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE dated 4/11/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-16,18-20 and 22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-16,18-20 and 22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/12/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 11, 2008 has been entered.

2. Accordingly Claims 1, 9, 15, 19, 23 and 36 has been amended. No new Claims were added. Therefore, Claims 1, 3-11, 13-16, 18-20 and 22-36 remain pending in the application. It also includes remarks and arguments.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**plurality of programmable resistive elements programmable by selective activation of at least one individual programmable resistive element**" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 9, 15, 19 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 1, 9, 15, 19 and 23 recites "a voltage threshold detector comprising a plurality of programmable resistive elements programmable by selective activation of at least one individual programmable resistive element" is indefinite because it is not clear

how the programmable resistive element of the voltage threshold detector is programmed. Particularly, looking at Fig. 3 and the specification, page 10, ll. 22-30, discloses the voltage threshold detector (400) comprising a resistor (397) and the plurality of diodes (371-375) , however it doesn't disclose the way of programming the resistor (397) of the voltage threshold detector. Moreover, it is not clear when the programming process occurs, for example by manufacturing (i.e. the time of fabrication) or is the programming done in the field after the manufacturing by the user. Secondly, programming in the fabrication process can be done by a variety of ways including changing the dimensions of the resistive layer, or also it can be done by changing the regime of a transistor (i.e. FET's) which can play the role of a resistive element, etc. Therefore, as best understood by the Examiner the Examiner will interpret programming the resistive element as nothing but appropriately sizing the resistor value.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,946,177) in view Li (US 6,639,771).

9. Regarding claims 1, 9, 15, 19 and 23, Miller et al. in (Fig. 7), discloses an integrated circuit including electrical over stress shunt (col. 1, ll. 5-13) comprising:

a voltage threshold detector (325) comprising a programmable resistive element (326) which is sized to the appropriate resistive value (col. 10, ll. 14-17), said voltage threshold detector (325) to detect an electrical over stress event wherein a potential is measured between a higher potential power rail (305) and a lower potential ground rail (310) in excess of a predetermined voltage (col. 9, ll. 43-47); and

a switchable low resistance path (345) between said power rail (305) and said ground rail (310), said low resistance path being adapted to be switched ON for a duration of said electrical over stress event lasting significantly longer than 2 microseconds (col. 9, ll. 22-32; col. 10, ll. 1-24). Further, an explanation of the circuit in Fig. 7 will be explained. As long as the power supply rail (Vdd) experiences an electrical discharge event, the voltage threshold detector (325) comprising diode string (327) will be conductive which will turn on transistor (329) as well as switching p-channel transistor (322) on. The latter transistor (322) provides a positive bias to the gate of clamping transistor (345) therefore switching a low resistance path between power supply rail (305) and power supply rail (310). This conductive state of the clamping transistor (345) can last indefinite in time (i.e. 1000 or 4000 microseconds) as long as the over-voltage is present on the power supply rail (305). Therefore, the protection circuit can protect against electrical over stress conditions lasting longer than 2 microseconds.

Miller et al. does not explicitly disclose said electrical over stress event occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected.

Li discloses an Internet ESD-shunt diode protected by delayed external mosfet switch (abstract) wherein the electrical over stress event occurs during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected (col. 1, ll. 18-20 and col. 2, ll. 12-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the electrical protection circuit of Miller et al. in an environment such as hot-swapping for telecom/datacom applications as disclosed by Li because it would expand the marketing and manufacturing of Miller et al. electrical protection device.

10. Regarding claims 3, 4, 13, 18, 22 and 24 Miller et al. in view of Li discloses all the limitations recited above in claims 1, 9, 15, 19, and 23.

11. Regarding claim 5, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 1, further comprising:

a driver (Miller et al., Fig. 4, 179,180) between said voltage threshold detector (Miller et al, Fig. 4, 182,183 and col. 9, ll. 22-24) and said switchable low resistance path (Miller et al., Fig. 4, 195).

12. Regarding claim 6, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 5, wherein:

said driver comprises a series connection of a plurality of inverters (Miller et al, Fig. 4, 179,180 and col. 6, ll. 51-54).

13. Regarding claims 7 and 14, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1 and 9, wherein said switchable low resistance path comprises:

a MOSFET transistor (Miller et al., Fig. 7, 345).

14. Regarding claim 10, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 9, wherein: said integrated circuit is based on 3.3v technology (Miller et al., col. 11, 13-15).

15. Regarding claims 11, 16 and 20, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 9 and 15 and 19, wherein:

said predetermined threshold (Miller et al., col. 9, ll. 43-52) is at least 5.5 volts (Miller et al., col. 11, 13-15).

16. Regarding claims 31-35, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1,9,15,19 and 23, wherein:

one of said powered device and said unpowered device is a connector (Li, Fig. 2, 90 and col. 2, ll. 50-67).

17. Regarding claim 36, Miller et al. in view of Li discloses the method of providing robustness to an electrical circuit from an over stress event according to claim 15,

wherein: a current drawn in detecting said EOS condition is minimized (Miller et al., Fig. 7, 326, col. 10, ll. 12-16).

18. Claims 8 and 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,946,177) in view of Li (US 6,639,771) as applied to claims 1 and 23 above, and further in view of Whitney et al. (US 2002/0024791).

19. Regarding claims 8 and 25, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1 and 23, wherein: said integrated circuit includes a interfaces for telecom and datacom applications (Li, col. 1, ll. 18-20 and col. 2, ll. 12-16).

Miller et al. and Li do not explicitly disclose a Firewire IEEE 1394 interface.

Whitney et al. discloses an electrostatic shunt circuit (abstract and para. [0002]) to protect an integrated circuit including a Firewire IEEE 1394 interface (Figs. 13A, B and page 6, para. [0093], ll. 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the protection circuit of Miller et al. mentioned combination in the Firewire interface of Whitney et al. to protect the input/output signals thereby improving the accessibility of the connections to the transmission lines and other lines of data transfer interfaces.

20. Regarding claims 26-30, Miller et al. in view of Li and in view of Whitney discloses the integrated circuit including an electrical over stress shunt according to claims 1,9,15,19 and 23, wherein:

one of said powered device and said unpowered device is a cable (Whitney et al. page 2, para, [0030 and 0045 and 0092 and 0093].

Response to Arguments

21. Applicant's arguments with respect to claims 1, 3-11, 13-16, 18-20 and 22-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TERRENCE R. WILLOUGHBY whose telephone number is (571)272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

TRW
5/22/08